High-speed Card Reader Chip CH377

Datasheet

Version: V1.1

https://wch-ic.com

1. Overview

CH377 is an industrial-grade USB2.0 high-speed card reader control chip, which connects SD card, MMC card and FLASH chip with SPI interface to realize the conversion of storage media such as SD card, MMC card and FLASH into standard USB mass storage devices, that is, U disk.

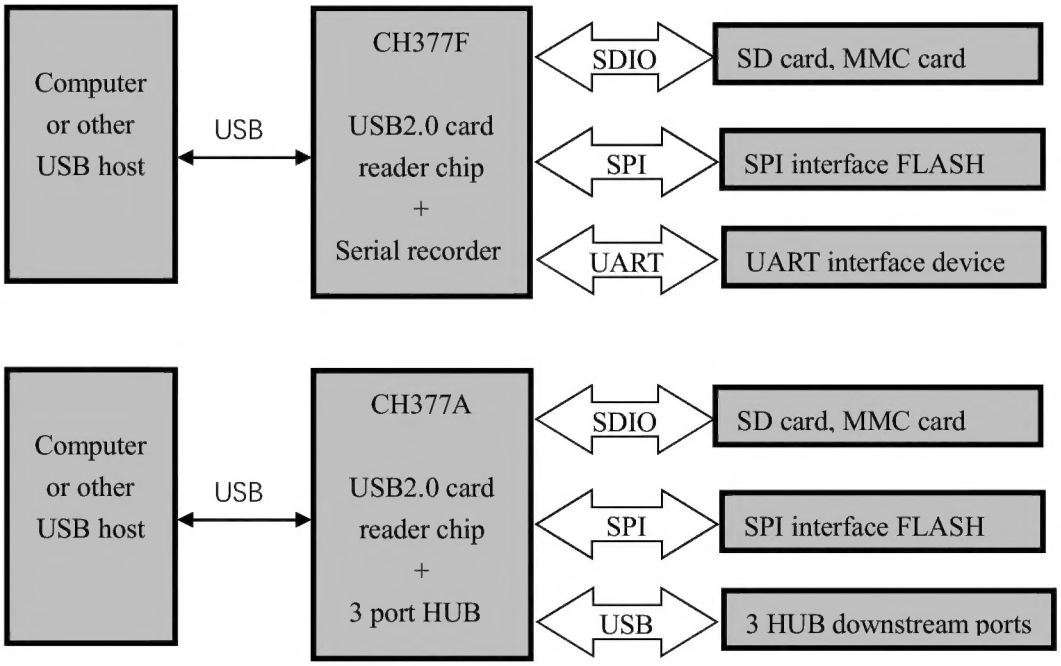
In addition to the USB2.0 card reader function, CH377A also has a 3-port USB2.0 high-speed HUB function. The upstream port supports USB2.0 high-speed and full-speed, and the downstream, port supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps.

CH377F supports serial recorder mode, which can receive serial data in real time and save it to storage media in the form of files.

CH377 adopts industrial-grade design, which can be applied to computer and industrial computer motherboards, docking stations, peripherals, embedded systems and other scenarios.

The following figure shows the application block diagram of CH377 chip.

Figure 1-1 Chip Application Block Diagram

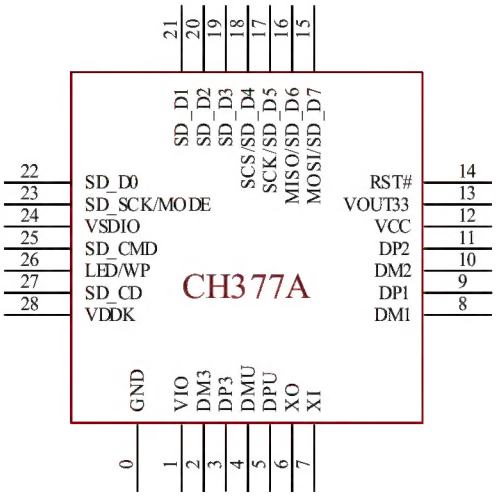


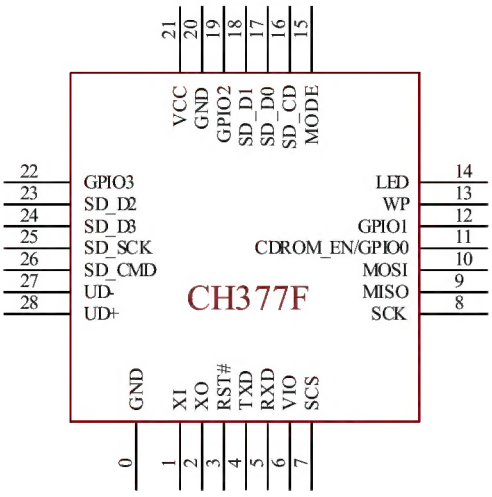
2. Features

- 480Mbps high-speed USB device interface, peripheral components only need crystal oscillator and capacitor.
- FLASH chip that supports SD/TF card, MMC card and SPI interface.
- Compatible with SD card specification 2.0, compatible with MMC specification 4.5.
- Single 3.3V power supply.
- CH377F supports serial port recorder mode, and saves serial port transparent transmission data in real time.
- CH377F supports the FAT file system and supports the configuration of parameters through configuration files.

- CH377F supports 4 GPIO input and output functions.
- CH377F serial communication baud rate supports 2400bps ~ 3000000bps.
- CH377A supports 3-port USB2.0 HUB function, provides 3 USB2.0 downstream ports, and is compatible with USB1.1 specification.
- The HUB function of CH377A supports high-performance MTT mode, and provides independent TT for each port to realize full bandwidth concurrent transmission.
- CH377A supports dual-disk function, with SD card or MMC card corresponding to disk 1 and SPI FLASH chip corresponding to disk 2.
- CH377A supports 4-wire or 8-wire SDIO mode, and CH377F only supports 4-wire SDIO mode.
- Built-in EEPROM, configurable chip VID, PID, maximum current, vendor and product information string and other parameters.
- Provide QFN28 no-lead package, compatible with RoHS.

3. Pinouts





Package Form	Body Size	Pin Pitch		Package description	Order Model
QFN28	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH377A
QFN28	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH377F

Note: 1. Pin 0# is the EPAD of QFN package and is a necessary connection.

2. The USB transceiver of CH377 is designed according to USB2.0, and the USB signal pin cannot be connected in series with resistors, otherwise the signal quality will be affected.

3. CH377A has a 3-port USB2.0 HUB function.

4. Pin Definitions

Table 4-1 CH377A pin definitions

Pin No.	Pin name	Type(1)	Function description
12	VCC	P	3.3V power supply input, external supply of 3.3V, it is recommended to connect an external 1uF in parallel to at least 22uF ground capacitance.
13	VOUT33	P	3.3V power output terminal, connected to the power input of SD card /MMC card.
28	VDDK	P	Core power supply, externally connected with 1uF capacitance to ground.
1	VIO	P	The power input of I/O port is externally connected with 0.1uF or 1uF capacitance to ground.
24	VSDIO	P	The decoupling end of internal power supply of SDIO pin is externally connected with 0.1uF capacitance to ground.
0	GND	P	The common ground terminal must be connected to GND.
14	RST#	I(FT)	External reset input, active low, built-in pull-up resistor.

4	DMU	USB	The upstream port USB2.0 signal line D- cannot be connected in series with additional resistors.
5	DPU	USB	The upstream port USB2.0 signal line D+ cannot be connected in series with additional resistors.
8	DM1	USB	1# Downstream port USB signal line D-.
9	DP1	USB	1# Downstream port USB signal line D+。
10	DM2	USB	2# Downstream port USB signal line D-。
11	DP2	USB	2# Downstream port USB signal line D+。
2	DM3	USB	3# Downstream port USB signal line D-。
3	DP3	USB	3# Downstream port USB signal line D+。
7	XI	I	The crystal oscillation input end is connected to one end of the external 20MHz crystal.
6	XO	O	The crystal oscillation inverting output end is connected to the other end of the external 20MHz crystal.
27	SD_CD	I(FT)	The SD card /MMC card is inserted into the detection pin.
22	SD_D0	I/O	SDIO interface data pin 0.
21	SD_D1	I/O	SDIO interface data pin 1.
20	SD_D2	I/O	SDIO interface data pin 2.
19	SD_D3	I/O	SDIO interface data pin 3.
18	SCS/	O	SPI interface chip selection pin.
	SD_D4	I/O(FT)	SDIO interface data pin 4.
17	SCK/	O	SPI interface clock pin.
	SD_D5	I/O(FT)	SDIO interface data pin 5.
16	MISO/	I	SPI interface data input pin with built-in pull-up resistor.
	SD_D6	I/O(FT)	SDIO interface data pin 6.
15	MOSI/	O	SPI interface data output pin.
	SD_D7	I/O(FT)	SDIO interface data pin 7.
23	SD_SCK/ MODE	O	SDIO interface data pin 7.
		I	Single disk mode configuration pin: During power-on, this pin is used as the configuration pin. If an external pull-down resistor (typical 4K7) is detected, it will be configured in single disk mode, and the SPI interface FLASH chip will be used as the storage medium. Built-in pull-up resistor, default to dual-disk mode.
25	SD_CMD	I/O	SDIO interface command pin.
26	LED/ WP	O	Status output pin, active low: When the USB configuration is completed, it will output a low level, and the USB will flash quickly when there is data communication.

		I	Write protection configuration pin: This pin is used as a configuration pin during power-on, and is set to read-only/write-protected mode if an external pull-down resistor (typical 4K7) is detected. Built-in pull-up resistor allows write operation by default.

Table 4-2 CH377F pin definitions

Pin No.	Pin name	Type(1)	Function description
21	VCC	P	3.3V power supply input, external supply of 3.3V, it is recommended to connect an external 1uF in parallel to the ground capacitance of at least 3.3uF.
6	VIO	P	The power input of I/O port is externally connected with 0.1uF or 1uF capacitance to ground.
0,20	GND	P	The common ground terminal needs to be connected with the ground wire of USB bus.
3	RST#	I	External reset input, active low, built-in pull-up resistor.
28	UD+	USB	Directly connected to the D+ data line of USB bus, no additional resistors can be connected in series.
27	UD-	USB	Directly connected to the D- data line of USB bus, no additional resistors can be connected in series.
1	XI	I	The crystal oscillation input end is connected to one end of the external 12MHz crystal.
2	XO	O	The crystal oscillation invert output end is connected with that other end of the external 12MHz crystal.
16	SD_CD	I(FT)	The SD card /MMC card is inserted into the detection pin.
17(2)	SD_D0	I/O(FT)	SDIO interface data pin 0.
18(2)	SD_D1	I/O(FT)	SDIO interface data pin 1.
23	SD_D2	I/O(FT)	SDIO interface data pin 2.
24	SD_D3	I/O(FT)	SDIO interface data pin 3.
25	SD_SCK	O	SDIO interface clock pin.
26	SD_CMD	I/O	SDIO interface command pin.
7	SCS	O	SPI interface chip select pin.
8	SCK	O	SPI interface clock pin.
9	MISO	I(FT)	SPI interface data input pin, built-in pull-up resistor.
10	MOSI	O	SPI interface data output pin.
4	TXD	O	UART serial data output pin, idle state is high.
5	RXD	I	UART serial data input pin, built-in pull-up resistor.
11	CDROM_EN/	I(FT)	CDROM enable pin:

	GPIO0		As a configuration pin during power-on, if this pin detects that a pull-down resistor (typical 4K7) is connected externally, the USB mass storage device will be set to CDROM mode. Built-in pull-up resistor, default to USB flash drive mode.
		I/O(FT)	GPIO0, used for IO port input or output.
12	GPIO1	I/O(FT)	GPIO1, used for IO port input or output.
19	GPIO2	I/O(FT)	GPIO2, used for IO port input or output.
22	GPIO3	I/O(FT)	GPIO3, used for IO port input or output.
13	WP	I(FT)	Write protection detection pin, active low: If the pin detects an external pull-down resistor (typical 4K7) at power-on, it is set to read-only/write-protected mode. Built-in pull-up resistor allows write operation by default.
14	LED	O	Status output pin, active low: When the USB configuration is completed, it will output a low level, and if there is data communication between USB and serial port, it will flash quickly.
15	MODE	I(FT)	Mode selection pin, which will switch from card reader mode to serial recorder mode if it detects an external pull-down resistor (typical 4K7) at power-on. Built-in pull-up resistor, default to card reader mode.

Note 1: Pin type abbreviation explanation:

USB = USB signal pin; I = Signal input; O = Signal output;

P = Power or ground; FT = Tolerant 5V voltage.

Note 2: The power supply of pins 17 and 18 of CH377F chip comes from VCC, which is 3.3V signal level; The power supply of other pins comes from VIO, which is the signal level of 3.3V/2.5/1.8V matched with VIO.

5. Function Description

5.1 General Description

CH377 is an industrial-grade USB2.0 high-speed card reader controller chip, which supports the connection of SD card, MMC card and FLASH chip with SPI interface, and realizes the conversion of storage media such as SD card, MMC card and FLASH into standard USB mass storage devices such as U disk and CDROM.

VCC of CH377 chip is the input of power supply, which needs to be externally supplied with rated 3.3V power supply.

The VIO pin of CH377 chip is used to provide I/O power supply for I/O and RST pins, which supports the power supply voltage of 1.8V ~ 3.3V VIO should use the same power supply as the connected peripherals. USB signal pins such as UD+ and UD- use VCC power supply instead of VIO power supply.

CH377 chip has built-in power-on reset circuit. When the chip works normally, it needs to provide 20MHz(CH377A) or 12MHz(CH377F) clock signal to the XI pin. The clock signal can be generated by crystal frequency stabilization oscillation through the inverter built in CH377. The peripheral circuit of CH377A chip needs to connect a 20MHz crystal between XI and XO pins, XI pin is connected with a resistance of about 4M7, and XO pin is connected with a load capacitor of about 30pF. The peripheral circuit of CH377F chip needs to connect a 12MHz crystal between the XI and XO pins, and each pair of XI and XO pins is grounded with a load capacitor of about 20pF.

CH377 chip has built-in all peripheral circuits required by USB bus, including embedded USB controller and USB-PHY, serial matching resistor of USB signal line, 1.5K pull-up resistor required by Device, etc. USB signal pins such as UD+ and UD- should be directly connected to the USB bus.

5.2 CH377A Function Description

CH377A chip can connect SD card and MMC card through SDIO interface (including SD_D0, SD_D1, SD_D2, SD_D3, SD_D4, SD_D5, SD_D6, SD_D7, SD_SCK, SD_CMD and optional SD_CD pin). You can also connect FLASH chips through SPI interfaces (SCS, SCK, MISO and MOSI pins) to realize the conversion of storage media such as SD cards, MMC cards and FLASH chips into standard USB mass storage devices.

CH377A chip supports 4-wire (SD_D0-SD_D3) or 8-wire (SD_D0-SD_D7) SDIO mode, in which SD_D4-SD_D7 pin and SPI interface are shared. At the time of power-on, the SD_D4-SD_D7 pins are first configured as SPI interface functions, and whether the external SPI interface FLASH chip exists is detected. If it exists, it will automatically switch to 4-wire SDIO mode, if it does not exist, it will switch to 8-wire SDIO mode, and finally, it will automatically select 4-wire or 8-wire mode according to the connection between the inserted SD card and MMC card.

CH377A chip supports dual-disk function, SD card or MMC card is used as the storage medium of disk 1, and FLASH chip with SPI interface is used as the storage medium of disk 2. If the existence of an external SPI interface FLASH chip is detected at power-on and the external pull-down resistor is not detected at the MODE pin, the dual-disk function is enabled, otherwise, the single-disk function is enabled. Disk 2 is generally used to store product information, software or drivers when leaving the factory. If the CDROM function is enabled, the U disk mode can be switched to the CDROM optical disk mode.

5.3 CH377F Function Description

CH377F chip has 2 working modes: USB card reader and serial recorder. By default, it works in USB card reader MODE. If the mode pin detects an external pull-down resistor when it is powered on, it will switch to serial recorder mode.

In USB card reader mode, the chip can connect SD card and MMC card through SDIO interface (including SD_D0, SD_D1, SD_D2, SD_D3, SD_SCK, SD_CMD and optional SD_CD pin), or connect FLASH chip through SPI

interface (SCS, SCK, MISO and MOSI pin). The storage media such as SD card, MMC card and FLASH chip are converted into standard USB mass storage devices, and CH377F does not support dual-disk mode.

In the serial recorder mode, the chip receives the serial data in real time and saves it in the storage medium as a file. The storage medium can be SD card or MMC card. After connecting the computer through USB port, you can directly read, write, delete and copy files. When it is powered on for the first time, a new configuration file "CONFIG.TXT" will be created in the storage medium and the default configuration information will be written. Users can modify the configuration file according to their own needs, and reset the configuration information such as baud rate of serial communication, starting file name, maximum storage size of a single file, and whether to overwrite the old file circularly.

The serial data of CH377F includes 1 low-level start bit, 8 data bits and 1/2 high-level stop bits, which supports no check/odd check/even check. Support common communication baud rates: 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, etc. The allowable baud rate error of CH377 chip serial port receiving signal is not more than 2%, and the baud rate error of serial port sending signal is less than 1.5%.

5.4 Chip Parameter Configuration

The manufacturer identification code VID, product identification code PID and product information of CH377 can be customized when it is used in large quantities. In a small number of applications, you can use the official configuration tools to configure parameters. The parameters mainly include the manufacturer identification code VID, product identification code PID, maximum current value, BCD version number, manufacturer information and product information string descriptor.

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description		Min.	Max.	Unit
T_A	Ambient temperature during operation	CH377A	-40	105	°C
		CH377F	-40	85	°C
T_J	Junction temperature range	CH377A	-40	110	°C
		CH377F	-40	100	°C
T_S	Ambient temperature during storage		-40	125	°C
V_{CC}	Power supply voltage (VCC pin supplies power, GND pin is grounded)		-0.3	4.0	V
V_{IO}	I/O supply voltage (VIO pin supplies power, GND pin is grounded)		-0.3	4.0	V
V_{USB}	Voltage on USB signal pin		-0.5	3.8	V
V_{IOFT}	Input voltage on FT pin		-0.5	5.5	V
V_{IO3}	Input voltage on other pins		-0.5	V_{CC}+0.3	V
V_{ESDUSB}	ESD tolerant voltage of HBM on USB signal pin		6K		V
V_{ESDIO}	ESD tolerant voltage of HBM on other pins		2K		V

6.2 Electrical Parameters (Test conditions: T_A=25°C, V_{CC}=3.3V, VIO = 3.3V, no USB pin)

Name	Parameter Description		Min.	Typ.	Max.	Unit
V_{CC}	Power supply voltage (VCC pin supplies power, GND pin is grounded)		3.0	3.3	3.6	V
V_{IO}	VIO supply voltage of I/O pin.		1.7	3.3	3.6	V
I_{CC}	Power supply current when the chip works normally	CH377A		46		mA
		CH377F		48		
I_{SLP}	Deep sleep power supply current (excluding 1.5KΩ pull-up) Or: Self-sleep power supply current (not connected to USB host)	CH377A		320		uA
		CH377F		220		
V_{IL}	Low level input voltage	Standard I/O pin	0		0.8	V
		FT pin	0		0.8	V
V_{IH}	High level input voltage	Standard I/O pin	2.0		V_{IO}	V
		FT pin	2.0		5.0	V
V_{ILRST}	Low input voltage of RST# pin		0		0.8	V

V_{OL}	Low level output voltage	Sink current 5mA			0.4	V
V_{OH}	High level output voltage	Source current 5mA	V_{IO}-0.4			V
R_{PU}	Internal pull-up equivalent resistance		30	40	50	kΩ
R_{PD}	Internal pull-down equivalent resistance		30	40	50	kΩ
V_{LVR}	Voltage threshold of low voltage reset of power supply	CH377A	2.5	2.9	3.2	V
		CH377F	1.9	2.2	2.5	V

6.3 Timing Parameters (Test conditions: T_A = 25℃, V_{CC} = 3.3V, V_{IO} = 3.3V)

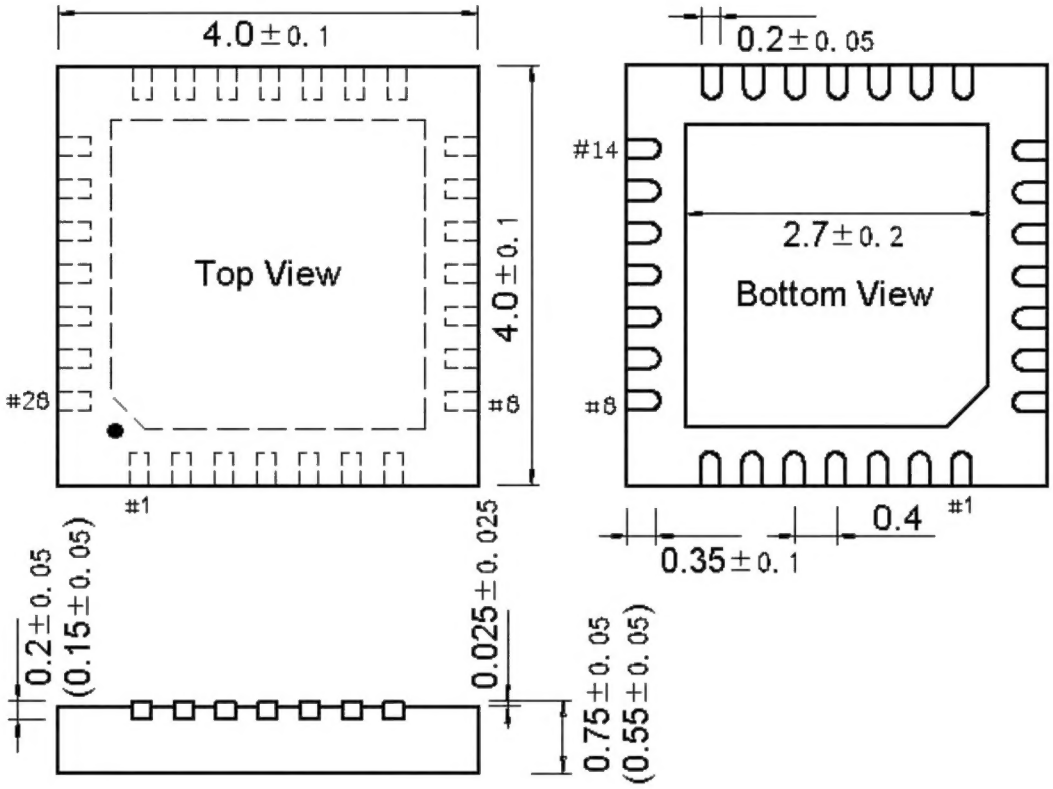
Name	Parameter Description	Min.	Typ.	Max.	Unit
TRSTD	Reset delay after power on or external reset input	15	28	40	mS
TSUSP	Detect USB automatic suspend time	3	5	9	mS
TWAKE	Chip awakening completion time after sleep	0.3	0.5	2	mS

7. Package Information

Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

7.1 QFN28

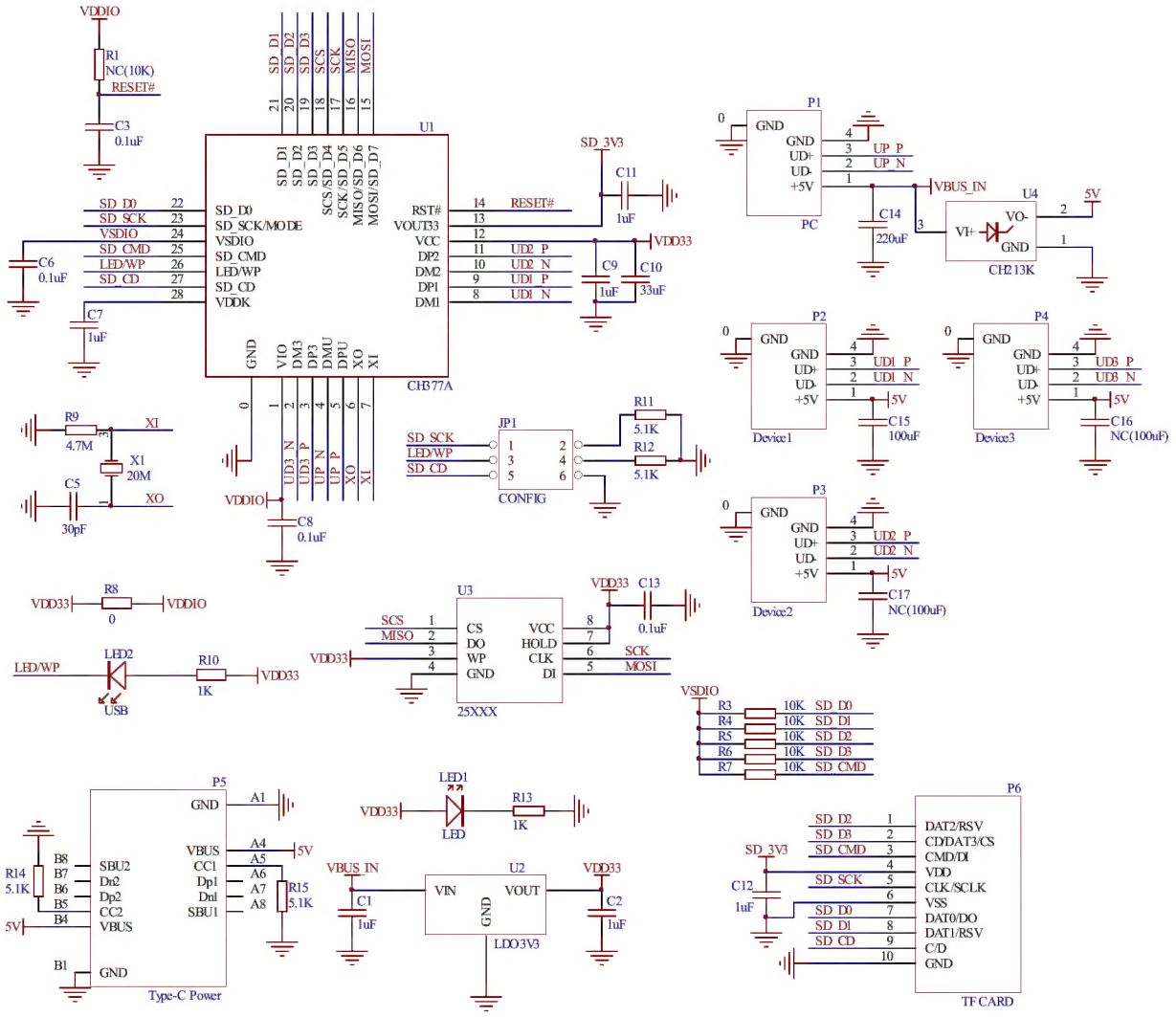


8. Applications

8.1 CH377A Chip Reference Circuit Diagram

Figure 8-1 is the reference circuit diagram of USB card reader +3-port USB2.0 HUB realized by CH377A chip.

Figure 8-1 CH377A application reference circuit diagram



P1 is the upstream USB interface of the HUB, P2-P4 are the 3 downstream USB interfaces of the HUB, P5 is the external auxiliary power supply interface, P6 is the SD card interface slot, which is used to connect SD cards or MMC cards, supports 8-wire MMC cards, and U3 is the FLASH chip with SPI interface.

When the HUB function is not used, the HUB-related components such as U4, P2-P4, P5, C14 and C15 can be removed.

U2 is an LDO linear voltage stabilizing chip with 5V to 3.3V. Try to choose a model with wide input range and low dropout. It is recommended that the load capacity should not be less than 500mA and there should be a cooling mechanism to ensure the output can be stabilized at 3.3V. U4 is an ideal diode CH213 with low voltage drop, which has simple over-current and short-circuit protection functions and faster protection response, and is used to avoid the backflow of VBUS_IN of the upstream port P1 from the P5 external power supply, especially when the upstream port such as the computer is turned off and the P5 external power supply is still available. Theoretically, U4 can be replaced by Schottky diode, but it is necessary to choose a device with low voltage drop, otherwise it will reduce

the output voltage of the downstream port VBUS. At a load current of 300mA, the voltage drop of Schottky diode is about 0.3V, and the voltage drop of ideal diode is about 0.05V.

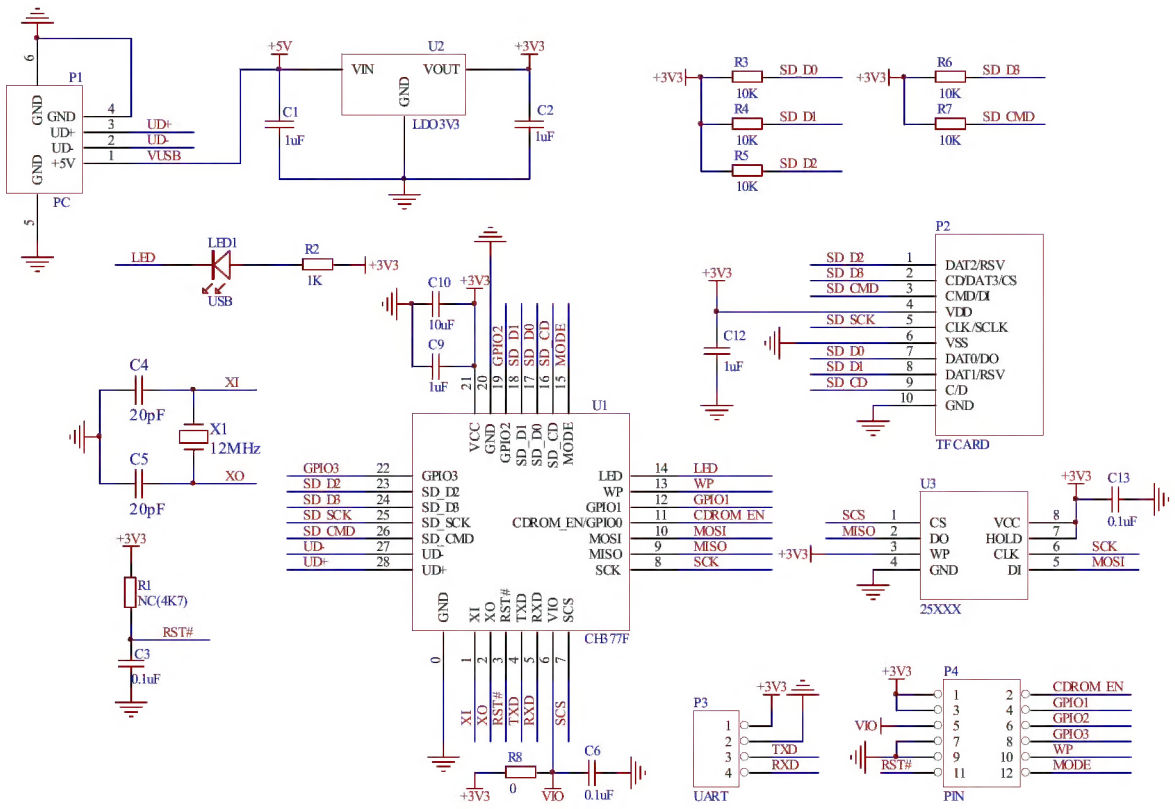
VOUT33 pin is used to provide controllable power supply for SD card or MMC card. It is suggested that the accumulated capacitance of VOUT33 pin should not exceed half the capacitance of VCC pin, otherwise the chip will be easily reset. Capacitors C9 and C10 are as close as possible to VCC pin of CH377A;

At the moment when the USB device in the downstream port of CH377A chip is hot-plugged, the dynamic load may cause the voltage of 5V to drop instantly, which may lead to the low-voltage reset of LVR, thus causing the phenomenon that the whole HUB is disconnected and reconnected. Improvement method: ①Increase the electrolytic capacitance of 5V power supply within the scope permitted by the specification (increase C14 capacity as shown in the figure) to alleviate the drop; ②Increase the capacitance at the input end of CH377 power supply (Increase C10 capacity as shown in the figure, for example, 47UF); ③Enhance the 5V power supply capacity or change to self-power supply. In addition, improving the quality of USB wire will also improve the power supply capacity.

8.2 CH377F Chip Reference Circuit Diagram

Figure 8-2 is the reference circuit diagram of USB card reader and serial recorder realized by CH377F chip.

Figure 8-2 CH377F application reference circuit diagram



P1 is a USB interface for connecting a USB host, P2 is an interface card slot for connecting an SD card or an MMC card, and U3 is a FLASH chip with SPI interface.

P3 is the serial TTL communication connection pin, which is used in parameter configuration or serial recorder mode. Includes 3.3V, GND, RXD and TXD pins. A level shifter (which must support high baud rate) can be added to realize the signal conversion from TTL to RS232, RS485 and RS422.

The VCC pin of CH377F chip is suggested to be externally connected with a power decoupling capacitor of 1uF in parallel with 10uF, as shown in C9 and C10 in the figure.
Crystal X1, capacitors C4 and C5 are used in the clock oscillation circuit of CH377F. The frequency of X1 is 12 MHz 0.4%, and C4 and C5 are high-frequency capacitors with a capacity of about 20pF. R1 and C3 are optional devices, and it is recommended to short VIO when RST# is not used.
It is suggested that the serial peripheral should use the same power supply as CH377, otherwise, the problem of IO pin backflow current should be considered when the power supply is separated.
When designing printed circuit board PCB, it should be noted that capacitors C9 and C10 should be as close as possible to VCC pin of CH377F; The D+ and D- signal lines of USB port are wired in parallel according to the high-speed USB specification, so as to ensure the characteristic impedance, and try to provide ground wires or copper-clad on both sides to reduce the signal interference from the outside.